THAT WHICH IS CLAIMED IS:

1. A method for the adjustment of a duration of an internal timing signal with a value close to a typical value of this duration, said method comprising the activation of said internal timing signal in said integrated circuit and of the sequential sending of the calibration values as an input of said integrated circuit, the expiration of the internal timing signal determining, as the calibration data of said integrated circuit, the last calibration value received or being received, said calibration data being applied to a device for adjusting the duration of said internal timing signal.

2. An adjustment method according to claim 1, wherein each calibration value corresponds to the ratio of the typical value to the total duration that has elapsed from the start of the internal timing signal to the time when this value is sent.

3. An adjustment method according to claim 2, wherein the adjustment device is pre-initialized at an initialization value.

4. An adjustment method according to claim 3, wherein each calibration value sent is assigned a factor corresponding to said initialization value.

5. An adjustment method according to any of the above claims, wherein the first calibration value is sent after a minimum duration of the internal timing signal has elapsed.

6. An adjustment method according to any of the above claims, said internal timing signal being a function of at least one reference given by a reference

circuit, wherein the adjustment device is applied to said reference circuit.

7. A method for the adjustment of a reference in an integrated circuit wherein said method consists in providing, in said integrated circuit, for a device for the adjustment of said reference on the basis of a piece of calibration data and a circuit for the generation of an internal timing signal from said reference and in applying a method of adjustment of the duration to the internal timing signal thus generated, so as to obtain the piece of calibration data to be applied to the device for adjusting said reference.

8. A method for the adjustment of a reference according to claim 7, wherein the adjusted reference circuit is a current source.

9. An adjustment method according to claim 7, wherein the adjusted reference circuit is a capacitor or a capacitor network.

10. A method for the adjustment of a reference according to any of the claims 7 to 9, wherein the piece of calibration data is applied to an adjustment device of another reference circuit having a structure identical to that of a reference circuit associated with said internal timing signal.

11. A method for the adjustment of a duration according to one of the above claims 1 to 6, applied to a non-volatile memory integrated circuit to adjust the duration of a signal for the programming of said memory

12. An adjustment method according to claim 11, comprising:

the launching of an operation of programming of any piece of data DXX at any address ADXX in the integrated circuit;

the successive sending, as data inputs, of calibration values of the integrated circuit,

the end of the programming of the piece of data that is any piece of data determining the last calibration value received or the calibration value that is being received by the integrated circuit as the calibration value.

13. An adjustment method according to claim 12 comprising, after the sending of all the calibration values defined for said internal timing signal as a function of the specifications of the integrated circuit, in launching a programming operation in the integrated circuit to program the piece of calibration data.

14. An adjustment method according to claim 12 or 13, wherein the piece of calibration data is programmed at a memory address determined internally to the integrated circuit.

15. An adjustment method according to claim 13 or 14 comprising, for the integrated circuit, in internally launching the programming of the piece of calibration data.

16. An adjustment method according to claim 13 or 14, wherein the integrated circuit receives a programming command of the piece of calibration data.

17. An adjustment method according to any of the claims 11 to 16, wherein the calibration values are recorded in a data input register of the integrated circuit.

18. An integrated circuit comprising a circuit for the generation of an internal timing signal from at least one reference and means for adjusting said reference, said adjustment means comprising temporary recording means for the recording of the data sent to a data input of the integrated circuit after an activation of said internal timing signal, a non-volatile memory element to store the data contained in said temporary storage means on the expiration of said internal timing signal and at least one adjustment device for the adjustment of a circuit for the generation of said reference, the data contained in said non-volatile memory element being applied to the input of said adjustment device.

19. An integrated circuit according to claim 18, comprising one or more reference circuits associated with the internal timing signal generation circuit, a first device for the adjustment of one of said reference circuits associated with the internal timing signal generation circuit and at least one second device for the adjustment of another reference circuit not associated with the internal timing signal generation circuit, the other reference circuit having a structure identical to one of the reference circuits associated with the internal timing signal generation circuit and a piece of data contained in the non-volatile memory element being applied to said first and second adjustment devices.

20. An integrated circuit according to claim 18 or 19 comprising a non-volatile memory, wherein the internal timing signal is the programming signal (PROG) of this memory and wherein the temporary storage means comprise a data input register.

21. An integrated circuit according to one of the claims 18 to 20, wherein an adjustment device is applied to a current reference circuit.

22. An integrated circuit according to one of the claims 18 to 20, wherein an adjustment device is applied to a capacitor or capacitor network type of reference circuit.

23. An integrated circuit according to one of the claims 18 to 20, wherein an adjustment device is applied to a resistor or resistor network type of reference circuit.

24. A system for the parallel testing of integrated circuits of one and the same technology, wherein said system comprises a table of calibration values of an internal timing signal of said integrated circuits to adjust the internal timing signal or at least one associated reference in each of said integrated circuits, by simultaneously applying to them an adjustment method according to any of the claims 1 to 17.